Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An interconnect substrate over which an interconnect pattern is formed, comprising:

a first portion having a rectangular body section; and

a second portion,

wherein the first portion has end parts as positioning references, the end parts formed by a plurality of projected sections that project from the rectangular body section and that lie in the same plane as the rectangular body section ; ~~and~~

wherein the second portion has such a shape that when the interconnect substrate is folded only at one boundary of the first and second portions, the second portion is superposed on and inside the first portion ~~except the end parts and is positioned between the end parts~~.

2. (Previously Presented) The interconnect substrate as defined in claim 1,

wherein each of the end parts as the positioning references includes two edges which are perpendicular to each other.

3. (Canceled)

4. (Currently Amended) The interconnect substrate as defined in claim ~~3,~~ 1,

wherein one of the projected ~~section~~ sections is a region determined by:

an edge which is a boundary between the projected section and the body section;

a first edge which is perpendicular to the edge as a boundary; and

a second top edge which is parallel to the edge as a ~~boundary,~~ boundary.

~~wherein one of the end parts as the positioning references includes the first and second edges.~~

5. (Original) The interconnect substrate as defined in claim 4,

wherein the body section of the first portion includes an edge having no projected section; and

wherein the second portion is disposed adjacent to the edge having no projected section.

6. - 9. (Canceled)

10. (Previously Presented) The interconnect substrate as defined in claim 1, wherein a plurality of holes are formed in the end parts.

11. (Previously Presented) The interconnect substrate as defined in claim 1, wherein the second portion continuously extends from the first portion.

12. (Previously Presented) The interconnect substrate as defined in claim 1, wherein the second portion is separated from the first portion; and

wherein the first and second portions are connected by the interconnect pattern.

13. (Currently Amended) A semiconductor device comprising:

at least one semiconductor chip; and

a substrate on which the semiconductor chip is mounted, the substrate having a first portion having a rectangular body section and ~~including~~ end parts as positioning references, the end parts formed by a plurality of projected sections that project from the rectangular body section and that lie in the same plane as the rectangular body section, the substrate having a second portion, the substrate folded at one boundary of the first and second portions to superpose the second portion on and inside the first ~~portion~~ portion, ~~except the end parts, the second portion positioned between the end parts,~~

wherein the second portion has a shape so as to be superposed on and inside the first portion ~~except the end parts~~ by folding the substrate only at the one boundary of the first and second portions.

14. (Original) The semiconductor device as defined in claim 13,

wherein a plurality of external terminals are provided in the first portion.

15. (Previously Presented) The semiconductor device as defined in claim 13,

wherein the interconnect substrate as defined in claim 1 is used as the substrate.

16. (Previously Presented) A circuit board on which is mounted the semiconductor device as defined in claim 13.

17. (Previously Presented) An electronic instrument provided with the semiconductor device as defined in claim 13.

18. (Previously Presented) A method of fabricating a semiconductor device, comprising the steps of:

mounting at least one semiconductor chip over the interconnect substrate as defined in claim 1; and

superposing the second portion on the first portion of the interconnect substrate.

19. (Previously Presented) A method of inspecting a semiconductor device, comprising the steps of:

positioning the semiconductor device as defined in claim 13 by using the end parts as the positioning references; and

inspecting electrical characteristics of the semiconductor device.

20. (Previously Presented) A method of mounting a semiconductor device comprising the steps of:

positioning the semiconductor device as defined in claim 13 by using the end parts as the positioning references; and

mounting the semiconductor device on a circuit board.